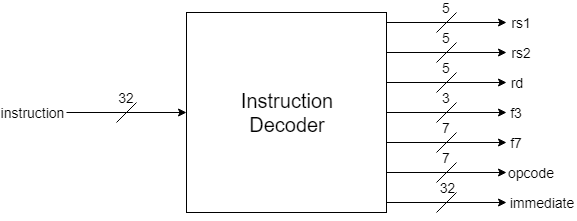
RISC-V ID

**RISC-V Instruction Decode Module**



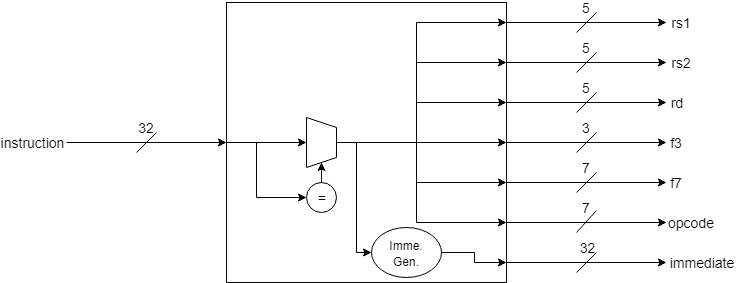
# Description

This is the RISC-V Processor’s instruction decode module. It receives the current instruction and checks it and extracts all the necessary information from it. The RISC-V ID checks if the instruction is all 1’s or all 0’s, this usually means that an empty memory chip has been connected. The RISC-V ID injects a “nop” instruction if this is the case, otherwise the instruction can be decoded. The information extracted includes the addresses of; the two registers than can be accessed by an instruction, the destination register, the “f3” code, the “f7 code”, the instruction opcode and the immediate number encoded in the instruction is decoded and sign-extended.

# Data Dictionary

|  |  |
| --- | --- |
| **Signal Name** | **Description** |
| instruction | Current instruction the processor is operating on |
| rs1 | Address of first register operand |
| rs2 | Address of second register operand |
| rd | Address of destination register operand |
| f3 | RISC-V specific function code |
| f7 | RISC-V specific function code |
| opcode | Instruction identifier code |
| immediate | Immediate number encoded in instruction |

# Implementation



There are two comparators present, one for all 1’s and one for all 0’s, the single bit output of both comparators is fed to an OR gate which feeds the mux present in the diagram, this mux’s inputs are tied to the “instruction” input or HEX “00000033” which is a “nop” instruction. Most of the required information is extracted directly from the instruction. However, the immediate number requires some minor circuitry to be extracted based on the type of instruction encoding being used i.e R,I,S,U,B,J. See the RISC-V specification Chapter 2 for further information on instruction and immediate value encoding.

# Revision History

* Revision 0.01 – Initial Revision, created document with block diagram, module description and data dictionary